Espressif: ECO and Workarounds for Bugs in ESP32

This document details the silicon errata for the ESP32

Errata

- When ESP32 is powered up or wakes up from Deep-sleep, a spurious watchdog reset occurs
- When the CPU accesses external SRAM through cache, sometimes random read and write errors occurs
- When the CPU accesses peripherals and writes one address repeatedly, random data loss occurs
- The Brown-out Reset (BOR) function is not functional. The system fails to boot up after BOR
- The CPU crashes when the clock frequency switches from 240 MHz to 80/160 MHz
- The pull-ups and pull-downs for the pads with both GPIO and RTC_GPIO functions can only be controlled by the RTC_GPIO registers. For these pads, the GPIO pull-up and pull-down configuration fields are non-functional
- There is a limit on the frequency range for the audio PLL

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