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Introduction

Recent advancements in successive-approximation-register analog-to-digital converters (SAR ADCs) have enabled much lower power consumption. These ADCs also maintain the resolution and sampling-rate performance that they are known for in the market. In general, SAR ADCs are faster than delta-sigma ADCs but often slower than pipeline ADCs. However, the resolution ranges of SAR ADCs are wider than the pipeline ADCs. In the current market, the resolution spectrum is fairly well covered, but there is a gap between the sampling speed of SAR ADCs and pipeline ADCs. The interleaving of SAR ADCs is a method of bridging this gap. Interleaving is a technique that enables a system to maintain the resolution of the SAR ADC while increasing the effective sample rate, helping bridge the speed gap. In an equivalent system, interleaved SAR ADCs can help reduce the overall power consumption, cost and size of the end system compared to pipeline ADCs. This article highlights some key considerations when designing an interleaved SAR ADC system and provides test results from an example system.